IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

NETLIST, INC., *Plaintiff*, v. SAMSUNG ELECTRONICS CO, LTD, *et al.* *Defendants*.	§ § § § § § § § §	CIVIL ACTION NO. 2:22-CV-00293-JRG (Lead Case)

NETLIST, INC., *Plaintiff*, v. MICRON TECHNOLOGY, INC., *et al.* *Defendants*.	§ § § § § § § § §	CIVIL ACTION NO. 2:22-CV-00294-JRG

CLAIM CONSTRUCTION MEMORANDUM OPINION AND ORDER

In these consolidated patent cases, Netlist alleges infringement by Samsung and Micron (and their affiliates) (together, "Defendants") of claims from four patents related to computer memory—U.S. Patent Nos. 7,619,912 (the "'912 Patent"); 9,858,215 (the "'215 Patent"); 10,268,608 (the "'608 Patent"); and 11,093,417 (the "'417 Patent"). The parties present ten disputes[1] about the proper construction of claim terms from the patents. Having considered the

[1] The parties briefed disputes for eleven claim terms, but Netlist has since withdrawn its assertion of a number of claims from the '912 Patent. *See* Joint Notice of Mootness Regarding Construction of Claims No Longer Asserted, Dkt. No. 201. As result, there is no longer a live dispute concerning one of the terms. *See id.* at 2–3.

parties' briefing and arguments of counsel during a September 26, 2023 hearing, the Court resolves the disputes as follows.

I. BACKGROUND

A. U.S. Patent 7,619,912

The '912 Patent relates "specifically to devices and methods for improving the performance, the memory capacity, or both, of memory modules." '912 Patent at 1:22–24. Generally, doubling the memory size of a DRAM[2] device more than doubles the associated cost. For example,

> by fabricating a 1-GB memory module using thirty-six 256-Mb memory devices [instead of 18 512-Mb devices], the cost of the resulting 1-GB memory module can be reduced since the unit cost of each 256-Mb memory device is typically lower than one-half the unit cost of each 512-Mb memory device. The cost savings can be significant, even though twice as many 256-Mb memory devices are used in place of the 512-Mb memory devices.

Id. at 4:51–58. "In other words, the price per bit ratio of the higher-density DRAM devices is greater than that of the lower-density DRAM devices." *Id.* at 4:62–64. Thus, under certain market conditions, there is an economic incentive for using pairs of lower-density DRAM devices instead of individual higher-density devices. *Id.* at 4:64–5:5.

The problem, however, is that a computer system may not be configured to provide the required control signals, like chip-select signals, for the lower-density chips. For example, a system expecting four ranks of memory might only provide two chip-select signals, but more are needed if replacing higher-density devices with lower-density devices. *See id.* at 7:20–35.

To address the problem, the patent teaches using a logic element, such as a programmable

[2] DRAM stands for "dynamic random-access memory." Stone Decl., Dkt. No. 129-6 ¶ 23. That the memory is "dynamic" means "the memory only remembers its information while power is maintained; if power is turned off, the contents of the DRAMs are lost." *Id.*

logic device (PLD), to "translate" the computer system's signals to signals appropriate for the lower-density memory devices. As an example, Table 1 shows a logic table for translating two chip-select signals and a row/column address signal from the computer (CS_0, CS_1, A_{n+1}) to four chip-select signals connected to the memory devices (CA_{0A}, CA_{0B}, CA_{1A}, CA_{1B}). *Id.* at 7:60–67.

The claims recite this "translation" functionality as responding to command and input signals from the computer by generating command and output signals to the memory devices. For example, Claim 1 recites:

> a circuit mounted to the printed circuit board, the circuit comprising **a logic element** and a register, **the logic element** receiving a set of input control signals from the computer system, the set of input control signals comprising at least one row/column address signal, bank address signals, and at least one chip-select signal, the set of input control signals corresponding to **a second number of DDR memory devices** arranged in a second number of ranks, the second number of DDR memory devices smaller than **the first number of DDR memory devices** and the second number of ranks less than the first number of ranks, the circuit generating a set of output control signals in response to the set of input control signals, the set of output control signals corresponding to the first number of DDR memory devices arranged in the first number of ranks, wherein *the circuit further responds to a first command signal and the set of input control signals from the computer system by generating and transmitting a second command signal and the set of output control signals to the plurality of memory devices*, the first command signal and the set of input control signals corresponding to the second number of ranks and the second command signal and the set of output control signals corresponding to the first number of ranks;

Id. at 32:66–33:23 (all emphasis added). The "second number of DDR memory devices" are the higher-density devices replaced by the lower-density "first number of DDR memory devices."

B. U.S. Patents 9,858,215 and 11,093,417

The ’215 and ’417 Patents have a common disclosure. Like the ’912 Patent, these patents relate “specifically to devices and methods for improving the performance, the memory capacity, or both, of memory modules.” ’215 Patent at 1:43–45; *see also* ’417 Patent at 1:48–50. Typically, DRAM is arranged in “ranks.” ’215 Patent at 2:41–47. During operation, those ranks are selected by address and command signals received from the processor, such as chip-select signals. *Id.* at 2:61–65.

As shown in FIG. 2 (below), in a conventional memory module, each memory device (30a, 30b) has data lines (DQa, DQb) and a strobe line (DQSa, DQSb). The data lines (102a, 102b) are connected to a common data line (112) and the strobe lines (104a, 104b) are connected to a common strobe line (114). This means the computer system is exposed to the loads of both memory devices at the same time, which can negatively affect performance. ’215 Patent at 6:60–7:13; *see also id.* at 9:43–45 (“increased load on the memory bus can degrade speed performance”).

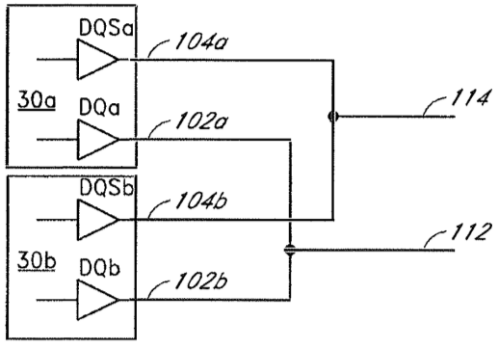

FIG. 2 of the ’215 and ’417 Patents

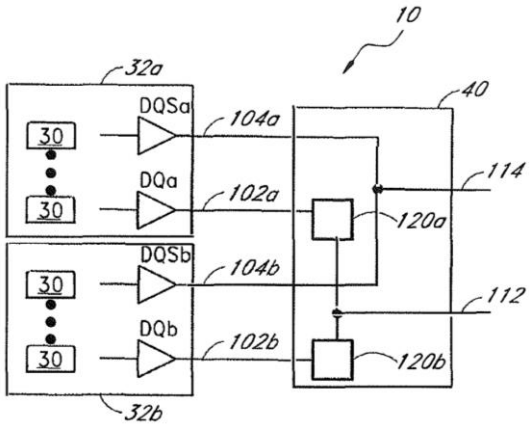

FIG. 4A of the ’215 and ’417 Patents

In contrast, FIG. 4A (above) shows a circuit (40) that “selectively isolates” the loads of the memory devices from the computer system. The circuit has a pair of switches (120a, 120b) on data lines (102a, 102b). Each switch can be actuated to selectively connect one or both data lines to a common data line (112). This allows a data signal to be transmitted from the memory controller to the memory devices of one or both ranks (32a, 32b) via the data lines (102a, 102b) and thereby isolate the memory devices when advantageous to do so. *See generally* ’215 Patent at 8:27–56.

Notably, these patents also include the subject matter of the ’912 Patent. Specifically, the description relating to FIGS. 9A–19 of the ’215 Patent and ’417 Patent is generally the same as the description of FIGS. 1A–14 of the ’912 Patent. The ’215 Patent and ’417 Patent add sections on “Load Isolation,” “Back-to-Back Adjacent Read Commands,” “Serial-Presence-Detect Device,” “Tied Data Strobe Signal Pins,” and “Memory Density Multiplication,” in addition to the ’912 Patent’s subject matter on “Command Signal Translation.” *See generally* ’215 Patent at 5:18–13:49, 17:41–37:9.

C. U.S. Patents 10,268,608

The ’608 Patent relates specifically to “multi-rank memory modules and methods of

operation." '608 Patent at 1:37–38. The patent teaches a memory module having memory devices, a module control circuit, and buffer circuits between respective sets of data signal lines in a data bus and respective sets of the memory devices. Each buffer circuit is positioned between a set of data lines and a set of memory devices. The buffer circuit buffers data signals in response to module control and clock signals. Each respective buffer circuit includes a delay circuit configured to delay the respective set of data signals by an amount determined based on at least one of the module control signals. '608 Patent at [57].

As far as claim construction is concerned, the parties only dispute whether the preamble of Claim 1 of the '608 Patent is limiting.

II. LEGAL STANDARDS

A. Claim Construction Generally

"[T]he claims of a patent define the invention to which the patentee is entitled the right to exclude." *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312 (Fed. Cir. 2005) (en banc). As such, if the parties dispute the scope of the claims, the court must determine their meaning. *See, e.g.*, *Verizon Servs. Corp. v. Vonage Holdings Corp.*, 503 F.3d 1295, 1317 (Fed. Cir. 2007) (Gajarsa, J., concurring in part); *see also Markman v. Westview Instruments, Inc.*, 517 U.S. 370, 390 (1996), *aff'g*, 52 F.3d 967, 976 (Fed. Cir. 1995) (en banc).

Claim construction, however, "is not an obligatory exercise in redundancy." *U.S. Surgical Corp. v. Ethicon, Inc.*, 103 F.3d 1554, 1568 (Fed. Cir. 1997). Rather, "[c]laim construction is a matter of [resolving] disputed meanings and technical scope, to clarify and when necessary to explain what the patentee covered by the claims . . . ." *Id.* A court need not "repeat or restate every claim term in order to comply with the ruling that claim construction is for the court." *Id.*

When construing claims, "[t]here is a heavy presumption that claim terms are to be given

their ordinary and customary meaning." *Aventis Pharm. Inc. v. Amino Chems. Ltd.*, 715 F.3d 1363, 1373 (Fed. Cir. 2013) (citing *Phillips*, 415 F.3d at 1312–13). Courts must therefore "look to the words of the claims themselves . . . to define the scope of the patented invention." *Id.* (citations omitted). The "ordinary and customary meaning of a claim term is the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention, i.e., as of the effective filing date of the patent application." *Phillips*, 415 F.3d at 1313. This "person of ordinary skill in the art is deemed to read the claim term not only in the context of the particular claim in which the disputed term appears, but in the context of the entire patent, including the specification." *Id.*

Intrinsic evidence is the primary resource for claim construction. *See Power-One, Inc. v. Artesyn Techs., Inc.*, 599 F.3d 1343, 1348 (Fed. Cir. 2010) (citing *Phillips*, 415 F.3d at 1312). For certain claim terms, "the ordinary meaning of claim language as understood by a person of skill in the art may be readily apparent even to lay judges, and claim construction in such cases involves little more than the application of the widely accepted meaning of commonly understood words." *Phillips*, 415 F.3d at 1314; *see also Medrad, Inc. v. MRI Devices Corp.*, 401 F.3d 1313, 1319 (Fed. Cir. 2005) ("We cannot look at the ordinary meaning of the term . . . in a vacuum. Rather, we must look at the ordinary meaning in the context of the written description and the prosecution history."). But for claim terms with less-apparent meanings, courts consider "those sources available to the public that show what a person of skill in the art would have understood disputed claim language to mean . . . [including] the words of the claims themselves, the remainder of the specification, the prosecution history, and extrinsic evidence concerning relevant scientific principles, the meaning of technical terms, and the state of the art." *Phillips*, 415 F.3d at 1314.

B. Means-Plus-Function Claiming[3]

A patent claim may be expressed using functional language. *See* 35 U.S.C. § 112 ¶ 6 (pre-AIA); *Williamson v. Citrix Online, LLC*, 792 F.3d 1339, 1347–49 & n.3 (Fed. Cir. 2015) (en banc in relevant portion). Under 35 U.S.C. § 112 ¶ 6, a structure may be claimed as a "means . . . for performing a specified function," and an act may be claimed as a "step for performing a specified function." *Masco Corp. v. United States*, 303 F.3d 1316, 1326 (Fed. Cir. 2002). When it applies, § 112 ¶ 6 limits the scope of the functional term "to only the structure, materials, or acts described in the specification as corresponding to the claimed function and equivalents thereof." *Williamson*, 792 F.3d at 1347.

However, § 112 ¶ 6 does not apply to all functional claim language. There is a rebuttable presumption that § 112 ¶ 6 applies when the claim language includes "means" or "step for" terms, and a rebuttable presumption it does *not* apply in the absence of those terms. *Masco Corp.*, 303 F.3d at 1326; *Williamson*, 792 F.3d at 1348. These presumptions stand or fall according to whether one of ordinary skill in the art would understand the claim with the functional language to denote sufficiently definite structure or acts for performing the function in the context of the entire specification. *See Media Rights Techs., Inc. v. Capital One Fin. Corp.*, 800 F.3d 1366, 1372 (Fed. Cir. 2015) (noting § 112 ¶ 6 does not apply when "the claim language, read in light of the specification, recites sufficiently definite structure" (quotation marks omitted) (citing *Williamson*, 792 F.3d at 1349; *Robert Bosch, LLC v. Snap-On Inc.*, 769 F.3d 1094, 1099 (Fed. Cir. 2014)));; *Masco Corp.*, 303 F.3d at 1326 (noting § 112 ¶ 6 does not apply when the claim includes an "act" corresponding

[3] Each of the patents has an effective filing date before the effective date of the Leahy-Smith America Invents Act, Pub. L. No. 112-29, § 3, 125 Stat. 284, 285-93 (2011). The Court therefore refers to the pre-AIA version of the statute.

to "how the function is performed"); *Personalized Media Commc'ns, LLC v. I.T.C.*, 161 F.3d 696, 704 (Fed. Cir. 1998) (noting § 112 ¶ 6 does not apply when the claim includes "sufficient structure, material, or acts within the claim itself to perform entirely the recited function . . . even if the claim uses the term 'means.'" (quotation marks and citation omitted)).

Construing a means-plus-function limitation involves multiple steps. "The first step . . . is a determination of the function of the means-plus-function limitation." *Medtronic, Inc. v. Advanced Cardiovascular Sys., Inc.*, 248 F.3d 1303, 1311 (Fed. Cir. 2001). "The next step is to determine the corresponding structure described in the specification and equivalents thereof. Structure disclosed in the specification is corresponding structure only if the specification or prosecution history clearly links or associates that structure to the function recited in the claim." *Id.* (citations and quotations omitted). The corresponding structure "must include all structure that actually performs the recited function." *Default Proof Credit Card Sys. v. Home Depot U.S.A., Inc.*, 412 F.3d 1291, 1298 (Fed. Cir. 2005). But § 112 does not permit "incorporation of structure from the written description beyond that necessary to perform the claimed function." *Micro Chem., Inc. v. Great Plains Chem. Co.*, 194 F.3d 1250, 1258 (Fed. Cir. 1999).

"[S]tructure can be recited in various ways, including [by using] 'a claim term with a structural definition that is either provided in the specification or generally known in the art,' or a description of the claim limitation's operation and 'how the function is achieved in the context of the invention.'" *Dyfan, LLC v. Target Corp.*, 28 F.4th 1360, 1366 (Fed. Cir. 2022) (quoting *Apple, Inc. v. Motorola, Inc.*, 757 F.3d 1286, 1299 (Fed. Cir. 2005)). For § 112 ¶ 6 limitations implemented by a programmed general-purpose computer or microprocessor, the corresponding structure described in the patent specification must usually include an algorithm for performing the function. *WMS Gaming Inc. v. Int'l Game Tech.*, 184 F.3d 1339, 1349 (Fed. Cir. 1999). In that case, the

corresponding structure is not a general-purpose computer but rather the special-purpose computer programmed to perform the disclosed algorithm. *Aristocrat Techs. Austl. Pty Ltd. v. Int'l Game Tech.*, 521 F.3d 1328, 1333 (Fed. Cir. 2008).

C. Indefiniteness

"[A] patent is invalid for indefiniteness if its claims, read in light of the specification delineating the patent, and the prosecution history, fail to inform, with reasonable certainty, those skilled in the art about the scope of the invention." *Nautilus, Inc. v. Biosig Instruments, Inc*., 572 U.S. 898, 901 (2014). The claims "must be precise enough to afford clear notice of what is claimed" while recognizing that "some modicum of uncertainty" is inherent due to the limitations of language. *Id.* at 908.

"Indefiniteness must be proven by clear and convincing evidence." *Sonix Tech. Co. v. Publ'ns Int'l, Ltd.*, 844 F.3d 1370, 1377 (Fed. Cir. 2017). And in the context of § 112 ¶ 6, "[t]he party alleging that the specification fails to disclose sufficient corresponding structure must make that showing by clear and convincing evidence." *TecSec, Inc. v. IBM*, 731 F.3d 1336, 1349 (Fed. Cir. 2013) (quoting *Budde v. Harley-Davidson, Inc*., 250 F.3d 1369, 1380–81 (Fed. Cir. 2001)).

III. THE LEVEL OF ORDINARY SKILL IN THE ART

The level of ordinary skill in the art is the skill level of a hypothetical person who is presumed to have known the relevant art at the time of the invention. *In re GPAC*, 57 F.3d 1573, 1579 (Fed. Cir. 1995). In resolving the appropriate level of ordinary skill, courts consider the types of and solutions to problems encountered in the art, the speed of innovation, the sophistication of the technology, and the education of workers active in the field. *Id.* Importantly, "[a] person of ordinary skill in the art is also a person of ordinary creativity, not an automaton." *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 421 (2007).

Only Micron offers, through its expert's declaration, a level of ordinary skill in the art for consideration. According to Micron's expert, a skilled artisan at the time of invention for the '215 and '417 Patents

> would have been someone with an advanced degree in electrical or computer engineering and at least two years working in the field, or a bachelor's degree in such engineering disciplines and at least three years working in the field. Such a person would have been knowledgeable about the design and operation of computer memories, most particularly DRAM and SDRAM devices that were compliant with various standards of the day, and how they interact with other components of a computer system, such as memory controllers. He or she would also have been familiar with the structure and operation of circuitry used to access and control computer memories, including sophisticated circuits such as ASICs and CPLDs and less sophisticated circuits such as tri-state buffers, flip flops, and registers.

Stone Decl., Dkt. No. 144-3 ¶ 21. Since no other party challenges that proposed level of skill, the Court adopts it for analysis of the disputed terms.

IV. THE DISPUTED TERMS

A. "first number of DDR memory devices arranged in a first number of ranks" and "second number of DDR memory devices in a second number of ranks" ('912 Patent); "memory devices mounted on the printed circuit board and arranged in a plurality of N-bit wide ranks" ('417 Patent); "plurality of memory integrated circuits mounted on the printed circuit board and arranged in a plurality of ranks including a first rank and a second rank" ('215 Patent)

Netlist's Construction	Defs.' Construction
"a predetermined group of [DDR] memory devices on a memory module that can send or receive a fixed number of data bits via a fixed width data bus, in response to a read or write command and independently from other [DDR] memory devices on the memory module"[4]	"Rank" means "an independent set of one or more memory devices on a memory module that act together in response to command signals, including chip-select signals, to read or write the full bit-width of the memory module."

The parties present two disputes, each centered on the meaning of "rank." First, they dispute whether a "rank" of memory can have a single memory device. Second, they dispute whether a "rank" of memory must be capable of sending or receiving a fixed number of data bits via a fixed width data bus. *See* Dkt. No. 129 at 1.

1. Whether a rank of memory can be a single memory device

According to Netlist, a "rank" must include more than one memory device. Netlist first relies on JEDEC[5] standards at the time of the effective filing dates of the underlying applications, which require a rank of either 64 or 72 bits, but does not define devices wider than 16 bits. Dkt. No. 129 at 2–4. Netlist also relies on Micron's expert's testimony that "[i]n the past for this definition of a rank . . . it has been more than one chip." *Id.* at 2–3 (quoting Strone Depo. Tr., Dkt. No. 129-5 at 44:15–20). Netlist says the specification supports this conclusion by consistently referring to "ranks" as multiple memory devices (plural). *Id.* at 4.

Defendants counter with four reasons why the intrinsic evidence shows a "rank" can be a single memory device. First, the '215 Patent describes and claims "*at least one* first memory

[4] Netlist's proposed construction for the '912 Patent includes the reference to "DDR." *See* Joint Cl. Constr. Chart, Dkt. No. 160-1 at 1 (Term 1). Also, Netlist's proposed construction for the '215 Patent uses "memory integrated circuits" rather than "memory devices." *Id.* at 8 (Term 14).

[5] JEDEC, or the Joint Electron Device Engineering Council, sets specifications for semiconductor memory circuits.

integrated circuit in [a] first rank and *at least one* second memory integrated circuit in [a] second rank," suggesting the possibility of a one-device rank. Dkt. No. 143 at 2 (citing '215 Patent at 3:31–35, 37:34–38; emphasis added). Second, Claim 55 of the '912 Patent recites "each rank . . . comprises a plurality of DDR DRAM chip packages," so if "rank" requires more than one memory device this phrase is superfluous. *Id.* Third, the specification repeatedly contemplates memory modules with two memory devices arranged in two ranks, one device in each rank. *Id.* at 2–3 (citing, *inter alia*, Figure 6A of the '912 Patent). Finally, cited prior art defines a "rank" as having *one or more* memory devices. *Id.* at 3 (quoting U.S. Patent 6,982,892 at 2:60–61 (emphasis added)).

Regarding Netlist's *extrinsic* evidence, Defendants call it unnecessary in light of the *intrinsic* evidence and "untethered to the asserted patents or their priority dates." *Id.* at 4–5. Regardless, it notes one treatise from around the time of the invention states "a rank of memory is a 'bank' of *one or more* DRAM devices that operate in lockstep in response to a given command." *Id.* at 5 (citing Bruce Jacob et al., *Memory Systems: Cache, DRAM, Disk* (2007), Dkt. No. 129-19 at 413 (emphasis added)).

The Court agrees with Defendants. As Jacob explains:

> In modern memory systems, multiple DRAM devices are commonly grouped together to provide the data bus width and capacity required by a given memory system. For example, 18 DRAM devices, each with a 4-bit-wide data bus, are needed in a given rank of memory to form a 72-bit-wide data bus. In contrast, embedded systems that do not require as much capacity or data bus width typically use fewer devices in each rank of memory—*sometimes as few as one device per rank*.

Bruce Jacob et al., *Memory Systems: Cache, DRAM, Disk* (2007), Dkt. No. 129-19 at 414 (emphasis added). Although Netlist stresses the last sentence of this excerpt applies only to embedded systems, Dkt. No. 150 at 4, nothing to which Netlist refers suggests the ordinary meaning of "rank"

differs depending on the system's complexity. To the contrary, while a one-device rank may be more likely found in an embedded system rather than a personal computer or server, Jacob shows the ordinary meaning of "rank" applies to both types of systems.

Other evidence supports this conclusion. For one, Jacob's definition is consistent with the PTAB's preliminary construction in a decision granting *inter partes* review of the '215 Patent. *See* Dkt. No. 143-3 at 12 ("On this preliminary record, we determine that the intrinsic evidence supports Petitioner's position that a rank may have only one memory device."). Perhaps most persuasively, Netlist itself previously stated a "rank" can be a single device. *See* App. Br., Dkt. No. 143-23 at 7 (noting that, in FIG. 2 of U.S. Patent 7,881,150, "each 'rank' includes only a single memory device"[6]).

Netlist's best argument relates to the JEDEC standards at the time, but it is still not persuasive. Those standards require a rank of 64 or 72 bits, but do not define DDR memory greater than 16 bits. *See* Dkt. No. 129 at 2. Thus, simple math suggests there will never be a rank consisting of only one memory device in an embodiment using that standard. That, however, does not alter the ordinary meaning of "rank" as used in the claims. Accordingly, the Court concludes a "rank" can include a single memory device.

2. Netlist's "fixed width data bus" requirement and "partial read" capability

Netlist claims the parties disagree about how a skilled artisan would determine which memory devices on a memory module belong to a particular rank. Dkt. No. 129 at 7. To help in that regard, Netlist asserts each "rank" is associated with its own chip-select signal and outputs or receives data via a "fixed width" bus, and "[n]othing in the '912 patent suggests . . . a rank of memory

[6] FIG. 2 of the '150 Patent is identical to FIG. 2 of the '215 and '417 Patents).

devices refers to a group of memory devices that is dynamically reconstituted to account for the changing memory bit width." *Id.* at 7–8. According to Netlist, "a POSITA would understand that a 'rank' must have the capability to send or receive the full bit-width of the memory module, but need not always do so." *Id.* at 9. Defendants question why this dispute matters, but nonetheless note the "patents contemplate 'increasing the number of memory devices per rank.'" Dkt. No. 143 at 6 (citing '912 Patent at 2:24–27).

To start, the Court agrees with Netlist that nothing in the patent suggests a changing memory bit width for a particular embodiment. The language to which Defendants point simply compares different memory modules to one another. *See* '912 Patent at 2:27–30 ("For example, a memory module with four ranks has double the memory capacity of a memory module with two ranks and four times the memory capacity of a memory module with one rank.").

That said, Netlist's proposed construction on this issue is too light on structure and too heavy on "capabilities." "Rank" has a clear structural definition, and the Court need not resolve the various capabilities the embodiments may or may not have because of that structure. As such, the Court declines to adopt Netlist's "fixed width data bus" language and "partial read" capability as not sufficiently tied to structure. *See Hewlett-Packard Co. v. Bausch & Lomb Inc.*, 909 F.2d 1464, 1468 (Fed. Cir. 1990) ("Apparatus claims cover what a device *is*, not what a device *does*.").

Finally, the Court rejects Defendants' proposed language of "in lockstep" as potentially confusing to a jury for those cases in which a "rank" comprises only one device. The Court, however, agrees that, in embodiments with ranks having more than one memory device, those devices operate together. With that in mind, the Court construes "rank" in these terms as "a 'bank' of one or more devices on a memory module that operate in response to a given signal."

B. "[row/column] address signal" ('912 Patent, all claims)

Netlist's Construction	Defs.' Construction
Plain and ordinary meaning.	"a varying electrical impulse that conveys an address of either a row or a column of memory locations from one point to another"

Each claim requires "a logic element . . . receiving a set of input control signals from the computer system, the set of input control signals comprising at least one row/column address signal . . . ." '912 C1 Patent at 1:33–36 (Claim 1)[7]; *see also id.* at 2:27–30 (Claim 15), 3:53–56 (Claim 28), 4:47–52 (Claim 39). The parties dispute whether the address signals can include "packetized control and address information" that is decoded by logic into output signals.

Defendants take a two-step approach to reach their construction. First, they point to a previously agreed-to construction for "signal" from earlier litigation. *See* Dkt. No. 143 at 9. Then they *assume* the agreed-to construction includes "packetized" signals and claim "Netlist offers no construction that would exclude 'packetized' signals and identifies no disclaimer or lexicography that would justify such a construction." *See id.* at 10.

Defendants' argument concerns Netlist's assertion, in 2009, of the '912 Patent against Google in the United States District Court for the Northern District of California. *See* Joint Cl. Const. & Prehr'g Statement, Dkt. No. 143-8. During that litigation, the parties informed the court they agreed on the construction of "signal" as "a varying electrical impulse that conveys information from one point to another." *See id.*, Ex. A. Netlist then filed an IDS with the Patent Office citing that Joint Statement. Information Disclosure Statement (June 8, 2010), Dkt. No. 143-9 at 5 (Cite No. 92). Defendants argue filing the IDS with the Office constitutes disclaimer. Dkt. No. 143

[7] Referring to the *Inter Partes* Reexamination Certificate, Dkt. No. 129-1 at 43–50.

at 8 (citing *Golden Bridge Tech. Inc. v. Apple Inc.*, 758 F.3d 1362 (Fed. Cir. 2014)).

Netlist does not contest the IDS might be binding in certain circumstances, but argues no construction is necessary for the jury to understand the scope of "signal." Dkt. No. 129 at 13. Regardless, says Netlist, "[p]acketized information transfer is not an electrical impulse, i.e., a high or a low which translates into a 1 or 0," and "[t]he intrinsic record makes no reference to packetized transfer of information as being the same as signals." Dkt. No. 150 at 5–6.

The Court agrees with Netlist. Rather than presenting the underlying dispute to the Court—here, whether "[row/column] address signal" includes "packetized" signals—Defendants point to a 2010 agreed construction that resolved a *different* dispute—"whether types of signals (e.g., command and control signals) needed to have 'pins of a device dedicated for that specific information.'" Dkt. No. 143 at 9 (citing Netlist's Open'g Cl. Constr. Br. (N.D. Cal.), Dkt. No. 143-12 at 9–13). Given the different disputes, that prior construction has no effect here.

If anything, based on the intrinsic record, Defendants must show why the ordinary meaning of "[row/column] address signal" *includes* packetized information. After all, the '912 Patent does *not* refer to packetized information for addressing. Nor do traditional DIMMS include "multiplex control and address information demuxed from the data." *See* Wolfe Depo. Tr., Dkt. No. 129-23 at 28:8–16. Because Defendants fail to present any evidence to the contrary, the Court rejects that the scope of the disputed term includes "packetized" signals. Otherwise, the Court will give this term a "plain and ordinary meaning" construction.

C. "A memory module connectable to a computer system, the memory module comprising" ('912 Patent, preamble of all asserted claims);

"A memory module operable to communicate with a memory controller via a memory bus, the memory bus including signal lines, the signal lines including

a set of control/address signal lines and a plurality of sets of data/strobe signal lines, the memory module comprising:" ('608 Patent, Claim 1)

Netlist's Construction	Defs.' Construction
Limiting preamble	Preamble not limiting

"In general, a preamble limits the invention if it recites essential structure or steps, or if it is 'necessary to give life, meaning, and vitality' to the claim. Conversely, a preamble is not limiting 'where a patentee defines a structurally complete invention in the claim body and uses the preamble only to state a purpose or intended use for the invention.'" *Catalina Mktg, Inc. v. Coolsavings.com, Inc.*, 289 F.3d 801, 808 (Fed. Cir. 2002).

Here, the preambles do not "only state a purpose or intended use for the invention." In fact, they state no purpose or intended use at all, instead requiring the memory module to be connectable to a computer system or operable to communication with a controller via a memory bus. As Micron's expert explains, "DRAM chips are mounted on small printed-circuit boards . . . typically referred to as memory modules." Stone Decl., Dkt. No. 129-6 ¶ 26. And "DRAM chips and the interfaces to the boards that include the DRAM chips, e.g., memory modules, are standardized so that memories from different vendors can be used in a variety of computers from different manufacturers." *Id.* ¶ 27.

Based in part on this explanation from Dr. Stone, the Court agrees with Netlist. The important concepts of a "small printed-circuit board" and "standardized interfaces" to computers are absent from the body of the claims. Thus, not only do the claims fail to recite a structurally complete invention, "[a] skilled artisan would understand a 'memory module' is distinct from, and has essential structural requirements not necessarily found in, other modular computer accessories[, including] the structure necessary to connect to a memory controller." Cl. Constr. Order (*Samsung*

I), Dkt. No. 129-7 at 28. Accordingly, the Court holds these are limiting preambles.

D. The Buffer Control Terms ('215 Patent, Claims 1, 21; '417 Patent, Claim 1)

Netlist's Construction	Def.' Constructions
These limitations do not require the first rank and second rank of memory integrated circuits to be on different forks.	"logic coupled to the buffer and configured to respond to the **first memory command** by providing first control signals **to selectively electrically couple the input of the buffer to a first data signal line at the output of the data buffer** to enable communication of the first data burst between the at least one first memory integrated circuit and the memory controller through the buffer, **and disabling a second data signal line at the output of the buffer connected to the second memory integrated circuit**" ('215 Patent, Claim 1)
	"wherein logic is further configured to respond to the **second memory command** by providing second control signals to **selectively electrically couple the input of the buffer to a second data signal line at the output of the data buffer** to enable communication of the second data burst between the at least one second memory integrated circuit and the memory controller through the buffer, **and disabling a first data signal line at the output of the buffer connected to the first memory integrated circuit**" ('215 Patent, Claim 1)
	"**a data buffer** coupled between the data signal lines in the N-bit wide memory bus and corresponding data pins of memory devices in each of the plurality of N-bit wide ranks, **the buffer configurable to selectively electrically couple a single data signal line at the input of the buffer to a first signal line and second signal line at the output of the buffer** to transfer N-bit wide data signals between the N-bit wide memory bus and the memory devices **in the one of the plurality of N-bit wide rank**, **wherein each signal line at the output of the buffer is connected to a different N-bit wide rank**" ('417 Patent, Claims 1, 6, 11)

Despite that the claims do not facially require enabling one data buffer while disabling other data buffers, Defendants argue the claims should be so limited based on the specification and

the prosecution history. Regarding the specification, Defendants point to the differences between FIG. 2 and FIG. 4A and characterize the invention as using a "fork-in-the-road" architecture for enabling load isolation. Dkt. No. 143 at 14. Defendants then stress allegedly disavowing statements made by Netlist in IPR proceedings for related patents in which Netlist characterized the ability to "selectively electrically couple" the memory controller to the data buffer as a key contribution of the inventions. *Id.* at 15–17.

According to Netlist, however, there is no such fork-in-the-road requirement. For one, says Netlist, FIGS. 8A and 8B show an embodiment without such an arrangement, suggesting a "fork in the road" is not essential to the invention. Dkt. No. 129 at 18–21, 23–24; Dkt. No. 150 at 8–9.

The Court agrees with Netlist. Regarding the specification, the Court rejects Defendants' assertion that "the only relevant disclosure . . . is directed to using a buffer to disable a data path for isolation." Dkt. No. 143 at 14. The "Load Isolation" section composes only part of the disclosures. *See* '215 Patent at 5:17–11:37. In fact, much of the disclosures repeat the subject matter of the '912 Patent—the translation of address and control signals from the computer system to memory modules using a logic element. *See id.* at 13:50–17:40. The disclosures also include sections on "Back-to-Back Adjacent Read Commands," *id.* at 12:37–13:49, "Serial-Presence-Detect Device[s]," *id.* at 17:41–30:3, and "Tied Data Strobe Signal Pins," *id.* at 30:5–37:9. The claims at issue include some subject matter from these other sections.[8] Thus, the Court is not convinced the

[8] For example, Claims 1 and 21 of the '215 Patent relate to memory commands that cause the memory module to receive or output data bursts, '215 Patent at 37:51–62, which the patent discusses under the "Back-to-Back Adjacent Read Commands" section, *see generally id.* at 11:39–13:50. Similarly, the last two limitations of Claim 1 of the '417 Patent concern CAS latency, '417 Patent at 42:54–67, which the patent discloses under the "Serial-Presence-Detect Device" section, *id.* at 22:36–62.

claims are directed only to the "load isolation" disclosure as opposed to other aspects of the patents.

Regarding Netlist's IPR statements, they specifically concerned the phrase "selectively electrically coupled" in the claims at issue, which Netlist clearly tied to the "Load Isolation" part of the disclosure. For example, Netlist had an entire section of its brief dedicated to explaining the importance of "load isolation." *See* App.'s Br., Dkt. No. 143-23 at 10–14. It explained:

> Adding the configurability to **selectively electrically couple** a device data line to a common data line was a key contribution of the inventions. When a memory device's data line is permanently electrically connected to the common data line, as is the case for both memory devices in the conventional memory module of FIG. 2, the computer system is always exposed to the electrical load of each such memory device on a module. But when a switch or other mechanism is used to **selectively electrically couple** the data lines, such as shown in FIG. 3A, the electrical load of the memory devices can be disconnected from the computer system by the switch. When the switch is not actuated, there is no electrical connection between the device data line and common data line, which means there is no electrical connection between the computer system (connected to the common data line) and the memory device (connected to the device data line). When that happens, the electrical load of the memory module is reduced to the load of the circuit 40 (*i.e.*, the switches and other components of the circuit, but not the memory devices).
>
> Solving the problem of increased loading due to additional memory devices was essential to overcoming the shortcomings of prior art memory modules.

Id. at 41–42 (emphasis added).

Here, however, the claims at issue use different language than "selectively electrically coupled" and, as discussed *supra*, are not so clearly tied to this "load isolation" concept to justify finding clear and unmistakable disclaimer. Accordingly, the Court rejects any fork-in-the-road requirement for these claims.

E. "logic" ('215 Patent, Claim 1; '417 Patent, Claim 1)

Netlist's Construction	Micron's Construction
Plain and ordinary meaning, not subject to § 112 ¶ 6.	Subject to § 112 ¶ 6, but there is no disclosure of adequate structure or algorithm for the functions of: <u>For Claim 1 of the '417 Patent</u> "output[ting] data buffer control signals in response to the read or write memory command" <u>For Claim 1 of the '215 Patent:</u> "(i) respond[ing] to the first memory command by providing first control signals to the buffer to enable communication of the first data burst between the at least one first memory integrated circuit and the memory controller through the buffer; and (ii) further respond[ing] to the second memory command by providing second control signals to the buffer to enable communication of the second data burst between the at least one second memory integrated circuit and the memory controller through the buffer"

Claim 1 of the '417 Patent recites "[a] memory module operable in a computer system" comprising:

> a printed circuit board having a plurality of edge connections configured to be electrically coupled to a corresponding plurality of contacts of a module slot of the computer system; [and]
>
> logic coupled to the printed circuit board and configurable to receive a set of input address and control signals associated with a read or write memory command via the address and control signal lines and to output a set of registered address and control signals in response to the set of input address and control signal . . . .

'417 Patent at 42:7–22. The claims further require the input address and control signals to include registered chip-select signals that are either "active" or "non-active." *Id.* at 42:22–40. Claim 1 of the '215 Patent includes a similar "logic" limitation, but requires the "logic" to be connected to a buffer that itself is coupled between a memory integrated circuit and a memory bus. *See* '215

Patent at 37:47–62.

Pointing to *Williamson* and *Egenera, Inc. v. Cisco Sys.*, 972 F.3d 1367 (Fed. Cir. 2020), Micron argues "the 'logic' limitations are claimed in a purely functional manner and fail to recite sufficient structure for performing the claimed functionality." Dkt. No. 143 at 24–26. In *Egenera*, the court considered whether the phrase "logic to modify said received messages to transmit said modified messages to the external communication network and to the external storage network" was subject to § 112 ¶ 6. Egenera argued the recited "logic to modify" was structural because it was part of a "control node," but the court rejected that argument. *See Egenera*, 972 F.3d at 1374 ("Mere inclusion of a limitation within a structure does not automatically render the limitation itself sufficiently structural. . . . [T]he question is not whether 'logic' is utterly devoid of structure but whether the claim term recites sufficient structure to perform the claimed functions."). Egenera also argued the claim language defined the "inputs, outputs, connections, and operation" of the logic component, thus providing sufficiently definite structure, but the court also rejected that argument. *Id.* ("[T]he claims and specification provide no structural limitation to the 'inputs, outputs, connections, and operation' of the claimed 'logic to modify.'").

Here, the "logic" is distinguishable from *Egenera*'s "logic to modify." In *Egenera*, the appellant argued that "logic" denoted "software, firmware, circuitry, or some combination thereof." The district court called that definition "'so broad and formless as to be a generic black box for performing the recited computer-implemented functions.'" *Egenera*, 972 F.3d at 1374 (quoting the district court). As used in these claims, however, "logic" clearly connotes *physical* structure rather than software, as the claims require the "logic" to be coupled to either a printed circuit board (in the '417 Patent) or a buffer (in the '215 Patent). Thus, "logic" here is not so "broad and formless" as the "logic to modify" of *Egenera*.

Moreover, the limitation requires connection of address and control signal lines, the receipt of address and control signals over those lines, and the output of chip-select signals based on the input signals. This is consistent with the specifications' disclosure of PLDs, ASICs, FPGAs, and CPLDs as "logic elements." *See, e.g.*, '417 Patent at 7:17–31 (noting that, "[i]n certain embodiments, the circuit [40] comprises a logic element selected from a group consisting of: a programmable-logic device (PLD), an application-specific integrated circuit (ASIC), a field-programmable gate array (FPGA), a custom-designed semiconductor device, and a complex programmable-logic device (CPLD)"). In light of that disclosure, and because a skilled artisan would have "been familiar with the structure and operation of circuitry used to access and control computer memories," Stone Decl., Dkt. No. 144-3 ¶ 21, the Court finds this limitation recites sufficiently definite structure to avoid invoking § 112 ¶ 6. Accordingly, this term will be given a "plain and ordinary meaning" construction.

F. "circuitry" ('417 Patent, Claims 1, 6, 11)

Netlist's Construction	Micron's Construction
Plain and ordinary meaning, not subject to § 112 ¶ 6	Subject to §112, ¶ 6, but there is no disclosure of adequate structure or algorithm for the function of "transfer[ring] the burst of N-bit wide data signals between the N-bit wide memory bus and the memory devices in the one of the plurality of N-bit wide ranks in response to the data buffer control signal"

Claim 1 recites:

> circuitry coupled between the data signal lines in the N-bit wide memory bus and corresponding data pins of memory devices in each of the plurality of N-bit wide ranks, the circuitry being configurable to transfer the burst of N-bit wide data signals between the N-bit wide memory bus and the memory devices in the one of the plurality of N-bit wide ranks in response to the data buffer control signals and in accordance with an overall CAS latency of the memory module[.]

'417 Patent at 42:54–62. Claims 6 and 11 further limit the "circuitry" to include "logic pipelines" and "data paths," respectively. *See id.* at 43:19–22 (Claim 6), 44:10–14 (Claim 11). Micron contends "circuitry" is governed by 35 U.S.C. § 112 ¶ 6 but is indefinite for lack of corresponding structure. Dkt. No. 143 at 28–30.

"[W]hen the structure-connoting term 'circuit' is coupled with a description of the circuit's operation, sufficient structural meaning generally will be conveyed to persons of ordinary skill in the art, and § 112 ¶ 6 presumptively will not apply." *Linear Tech. Corp. v. Impala Linear Corp.*, 379 F.3d 1311, 1320 (Fed. Cir. 2004). In *Linear Tech*, the court held the claims' recitation of the circuit's objective was sufficient to avoid invoking § 112 ¶ 6. *Id.* (noting "[t]he contextual language describes the objective of the 'circuit,' [which is] 'monitoring a signal from the output terminal,' and the desired output of the 'circuit,' [which is] 'generating a first feedback signal'").

Here, too, the claims at issue provide the objective and desired output of the circuit.

Specifically, Claim 1 recites "transfer[ring] the burst of N-bit wide data signals between the N-bit wide memory bus and the memory devices in the one of the plurality of N-bit wide ranks in response to the data buffer control signals and in accordance with an overall CAS latency of the memory module." '417 Patent at 42:57–62. Moreover, the claims recite registering data transfers through the circuitry "for an amount of time delay *such that* the overall CAS latency of the memory module is greater than an actual operational CAS latency of each of the memory devices." *Id.* at 42:64–67 (emphasis added). Given Micron's characterization of a skilled artisan as one "knowledgeable about the design and operation of computer memories, most particularly DRAM and SDRAM devices that were compliant with various standards of the day, and how they interact with other components of a computer system, such as memory controllers," Stone Decl., Dkt. No. 144-3 ¶ 21, the Court holds § 112 ¶ 6 does not apply and will give this term a "plain and ordinary meaning" construction.

G. "the at least one of the circuit components" ('215 Patent, Claim 15)

Netlist's Construction	Micron's Construction
Plain and ordinary meaning	Indefinite

This dispute relates to both Claim 14 and Claim 15 of the '215 Patent. The former requires the buffer of Claim 1 to include "circuit components configurable to provide a first data path or a second data path depending on whether the first rank or the second rank is selected to communicate data with the memory controller." '215 Patent at 39:24–28. Claim 15, which depends from Claim 14, then recites "the at least one of the circuit components is configured to provide the first data path in response to the first control signals, and is configured to provide the second data path in response to the second control signals." *Id.* at 39:29–33. Micron argues this phrase from Claim 15 has at least two possible and equally plausible meanings: (1) "wherein [[the]] at least

one of the circuit components is configured to provide . . .”; or (2) “~~the at least one of~~ the circuit components are configured to provide . . .” Dkt. No. 143 at 24. As such, Micron says, this phrase is indefinite. *Id.*

The Court disagrees. For one, there is no material difference in scope between Micron’s two proffered meanings. In other words, regardless of whether (1) “at least one of the circuit components” or (2) “the circuit components” are configured as required by the claims, those two phrases effectively mean the same thing. In addition, the only substantive limitation added by Claim 15 is the requirement that the provision of the data paths be “in response” to control signals. Thus, construing the phrase as “the circuit components” reflects how a skilled artisan would understand the term because it best aligns the language of Claim 15 with that of Claim 14. The Court therefore adopts that construction.

H. “burst of data strobe signals” (’215 Patent, Claims 12, 13, 28, 29)

Netlist’s Construction	Micron’s Construction
Plain and ordinary meaning.	Indefinite.

Claim 1 of the ’215 Patent is directed to

> [a] memory module operable in a computer system to communicate data with a memory controller of the computer system via a memory bus in response to memory commands received from the memory controller, the memory commands including a first memory command and a subsequent second memory command, the first memory command to cause the memory module to receive or output a first data burst and the second memory command to cause the memory module to receive or output a second data burst . . .

’215 Patent at 37:12–21. Claim 12, which depends from Claim 1, specifies:

> the first memory command is a first read command and the second memory command is a second read command, wherein the first read command and the second read command are back to back adjacent

> read commands, and wherein the memory module outputs the first data burst together with **a first burst of data strobe signals** in response to the first read command, wherein [the] memory module outputs the second data burst together with **a second burst of data strobe signals** in response to the second read command, wherein the second data burst follows the first data burst on the memory bus, and wherein the buffer is configured to prevent the **first burst of data strobe signals** and the **second burst of data strobe signals** from colliding with each other.

Id. at 39:1–14 (emphasis added).

Micron challenges this term as indefinite because the bursts could come from either "combined" or "non-combined" strobes. Dkt. No. 143 at 23. With "combined" strobes, two different memory devices have their strobe pins tied together. Stone Decl., Dkt. No. 144-3 ¶ 47. "Non-combined" strobes come from a single memory device. *Id.* ¶ 48. Netlist argues the term is broad enough to include both sources. Dkt. No. 129 at 26.

Micron focuses on the wrong question. Specifically, Micron looks to what *originates* the required "burst of data strobe signals," rather than the "bursts" themselves. The claims only require "the memory module [to] output[] the first data burst together with a first burst of data strobe signals." They say nothing about the underlying structural configuration that creates the "bursts." Thus, Micron at most shows the claims are indifferent as to the configuration of the *source* of the "bursts," and not what a "burst" is or is not. As such, it has not carried its burden on indefiniteness, and the Court will give this term a "plain and ordinary meaning" construction.

I. "operable in a computer system to communicate data" ('215 Patent, Claim 1; '417 Patent, Claim 1)

Netlist's Construction	Defs.' Construction
Plain and ordinary meaning	"configured in a computer system to communicate data"

Defendants question whether this term "requires mere capability (including after modification) or whether it requires structure that presently is configured to perform the recited function." Dkt. No. 143 at 20. They point to *TQ Delta, LLC v. CommScope Holding Co.*, No. 2:21-CV-309-JRG, 2022 WL 2071073 (E.D. Tex. June 8, 2022), in which the Court explained "'operable to' should be construed to refer to being configured to operate in the recited manner.'" *Id.* Netlist, however, asserts "[t]hat concern is not present here" because a skilled artisan "would understand that memory modules are designed to communicate data with a memory controller . . . without modification." Dkt. No. 129 at 27–28.

Based on the briefing, the parties apparently agree with the well-established principle "that a device capable of being modified to operate in an infringing manner is not sufficient, by itself, to support a finding of infringement." *See Telemac Cellular Corp. v. Topp Telecom, Inc.*, 247 F.3d 1316, 1330 (Fed. Cir. 2001). In other words, if the claims recite some structure "operable" to perform a task, an accused device must be *presently* "operable" to perform that task to infringe. Given the parties' apparent agreement on that point, the Court will give this term a "plain and ordinary meaning" construction.

J. "data buffer control signals" ('417 Patent, Claims 1, 3, 11)

Netlist's Construction	Defs.' Construction
Plain and ordinary meaning	"a signal sent to a buffer to selectively electrically couple the data signal line at the input of the buffer to a first signal line and a second signal line at the output of the buffer wherein each of the first signal line and the second signal line is connected to a different rank"

This term first appears near the end of the "logic" limitation of Claim 1. Specifically, the claim requires logic "configurable to output data buffer control signals in response to the read or write memory command." '417 Patent at 42:38–49.

Defendants base their construction on the limited disclosure of "control signals" in the specification. Dkt. No. 143 at 19 (noting the disputed term does not appear in the original specification). They suggest "[a]ny other construction 'would likely render the claims invalid for lack of written description.'" *Id.* (quoting *Ruckus Wireless, Inc. v. Innovative Wireless Sols., LLC*, 824 F.3d 999, 1004 (Fed. Cir. 2016)).

The Court disagrees for two reasons. First, Defendants' construction, which uses the phrase "selectively electrically couple," introduces the "fork-in-the-road" approach into the claims. *See* Dkt. No. 143 at 19 (arguing "Netlist cannot escape its prosecution statements that describe the invention as requiring a fork-in-the-road implementation"). The Court has already rejected that position. *See* Part IV.D. *supra*. Second, the Court is not persuaded mixing the claim-construction and written-description inquiries is proper on this record. In *Ruckus Wireless*, the Federal Circuit's decision hinged on first applying all the other rules of claim construction and still finding the term "ambiguous." *See Ruckus Wireless, Inc.*, 824 F.3d at 1004 ("If, after applying all other available tools of claim construction, a claim is ambiguous, it should be construed to preserve its validity."). Here, however, Defendants make no attempt to show "data buffer control signals" is ambiguous. See Dkt. No. 143 at 19. The Court will therefore give this term a "plain and ordinary meaning" construction.

K. "overall CAS latency [of the memory module]" ('417 Patent, Claim 1; '215 Patent, Claims 3, 4, 24, 25)

"actual operational CAS latency of each of the memory devices" ('417 Patent, Claim 1)

"actual operational CAS latency of each of the plurality the memory integrated circuits" ('215 Patent, Claims 3, 4)

"actual operational CAS latency of the memory integrated circuits" ('215 Patent, Claims 24, 25)

Netlist's Construction	Micron's Construction
Plain and ordinary meaning	**"overall CAS latency":** "The delay between: (1) the time when a read command is executed by the memory module, and (2) the time when the first piece of data is made available at an output of the memory module." **"actual operational CAS latency of each of the memory devices":** "the delay between: (1) the time when a read command is executed by each of the plurality of memory integrated circuits, and (2) the time when the first piece of data is made available at an output of each of the plurality of memory integrated circuits" **"actual operational CAS latency of each of the [plurality of] memory devices":** "the delay between: (1) the time when a read command is executed by the memory integrated circuits, and (2) the time when the first piece of data is made available at an output of the memory integrated circuits"

"CAS latency" means "column address strobe latency." As used in the claims, "overall CAS latency" refers to the "CAS latency" of a memory module, and "actual operational CAS latency" refers to the "CAS latency" of a memory device on the module. For example, Claim 1 of the '417 Patent requires:

> circuitry . . . configurable to transfer the burst of N-bit wide data signals between the N-bit wide memory bus and the memory

> devices in the one of the plurality of N-bit wide ranks in response to the data buffer control signals and in accordance with an **overall CAS latency** of the memory module;
>
> wherein data transfers through the circuitry are registered for an amount of time delay such that the **overall CAS latency** of the memory module is greater than an **actual operational CAS latency** of each of the memory devices.

'417 Patent at 42:54–67 (emphasis added). *See also* '215 Patent at 38:1–10 (reciting, in Claims 3 and 4, "overall CAS latency" and "actual operational CAS latency of each of [a] plurality of memory devices"); *id.* at 40:47–55 (reciting, in Claims 24 and 25, "overall CAS latency" and "actual operational CAS latency of . . . memory integrated circuits").

The parties generally agree "CAS latency" is a time between a command being executed and the presentation of data somewhere within the system, depending on the context of the surrounding language. For example, the parties agree the "overall CAS latency" of a memory module for a read command is the delay between (1) the time when the read command is executed by the memory module, and (2) the time when data is made available.[9]

The dispute concerns whether "CAS latency" refers *only* to "read" commands (Micron's position), or also to "write" commands (Netlist's position). According to Micron, the industry understood "CAS latency" at the relevant time as synonymous with "read latency." Dkt. No. 143 at 22. It accuses Netlist of trying to improperly broaden the meaning of "CAS latency." *Id.* at 23.

Netlist disagrees for three reasons. First, Netlist points to the claims, which it says support a construction that includes both "read" and "write" commands. Dkt. No. 129 at 29 (noting Claim 1 of the '417 Patent is expressly directed to both read and write commands and concerns "data

[9] Netlist's agreement is not explicit, but it does not challenge the structure of Micron's proposed construction—only that it is limited to "read" commands. *See* Dkt. No. 129 at 28–29.

transfers through the circuitry"). *Id.* Second, Netlist alleges Micron's construction would improperly exclude disclosed embodiments. *Id.* (citing '215 Patent at 20:22–47). Last, Micron's construction narrows the scope of the term's ordinary meaning without showing clear disavowal. *Id.* at 30.

The disclosure addresses "CAS latency" in only one paragraph:

> The circuit 40 comprises the SPD device 240 which reports the CAS latency (CL) to the memory controller of the computer system. The SPD device 240 reports a CL which has one more cycle than does the actual operational CL of the memory array. Data transfers between the memory controller and the memory module are registered for one additional clock cycle by the circuit 40. The additional clock cycle is added to the transfer time budget with an incremental overall CAS latency. This extra cycle of time advantageously provides sufficient time budget to add a buffer which electrically isolates the ranks of memory devices 30 from the memory controller 20. The buffer comprises combinatorial logic, registers, and logic pipelines. The buffer adds a one-clock cycle time delay, which is equivalent to a registered DIMM, to accomplish the address decoding. The one-cycle time delay provides sufficient time for read and write data transfers to provide the functions of the data path multiplexer/demultiplexer. Thus, for example, a DDR2 400-MHz memory system as described herein has an overall CAS latency of four, and uses memory devices with a CAS latency of three.

'215 Patent at 20:22–47 (cleaned up for easier reading).

Based on this paragraph, the Court agrees with Netlist. The disclosure explains the one-cycle time delay "provides sufficient time for *read and write data transfers* to provide the functions of the data path multiplexer/demultiplexer." '215 Patent at 20:39–42. Moreover, the disclosure refers to data transfers *between* the memory controller and the memory module" rather than in only one direction or the other. *Id.* at 20:27–29. Similarly, the claim limitations in which these terms appear refer to "caus[ing] the memory module to *receive or output*" a data burst, *id.* at 37:16–22 (emphasis added), and "data transfers *through* the circuitry," '417 Patent at 42:63 (emphasis added).

Regarding the extrinsic evidence, Micron's expert agrees "CAS latency can relate to both read and write data transfers." Stone Depo. Tr., Dkt. No. 129-5 at 76:16–18. And while Micron suggests "CAS latency" *usually* refers to "read latency," it also recognizes these "are not well-known terms of art." *See* Dkt. No. 143 at 22. Moreover, the parties agree "write latency" is closely related to "read latency." Dkt. No. 129 at 30 (citing JESD79-2, Dkt. No. 129-2 at 24); Dkt. No. 143 at 23 ("While CAS latency was only associated with Read Latency (RL) at the relevant time, Write Latency (WL) was a concept that was defined *in terms of* Read Latency.").

Based on the totality of the evidence, a skilled artisan would understand "CAS latency" includes both "read latency" and "write latency," depending on the context. The Court therefore rejects Micron's position and construes:

- **"overall CAS latency"** of a memory module as "the delay between: (1) the time when a command is executed by the memory module, and (2) the time when data is made available to or from the memory module";
- **"actual operational CAS latency"** of a memory device as "the delay between: (1) the time when a command is executed by the memory device, and (2) the time when data is made available to or from the memory device"; and
- **"actual operational CAS latency"** of a memory integrated circuit as "the delay between: (1) the time when a command is executed by the memory integrated circuit, and (2) the time when data is made available to or from the memory integrated circuit."

L. "wherein data transfers through the circuitry are registered for an amount of time delay such that the overall CAS latency of the memory module is greater than an actual operational CAS latency of each of the memory devices" ('417 Patent, Claim 1)

Netlist's Construction	Micron's Construction
Plain and ordinary meaning.	Indefinite

Micron contends this phrase is indefinite under either Netlist's or Micron's proposed

construction for "CAS latency." Dkt. No. 143 at 21. Under Micron's construction, which limits a "CAS latency" to a "read latency," "[i]t is nonsensical to 'register' data *to be written* 'for an amount of time delay'" that relates to a read latency. *Id.* And under Netlist's "apparent" construction, there would be no time delay for "overall CAS latency," which could then never be greater than the "actual operation CAS latency of the memory device." *Id.*

According to Netlist, the "conflict" Micron identifies with respect to its construction for "CAS latency" further supports the notion that term is not limited to a "read" latency. Dkt. No. 150 at 10. Netlist also notes Micron's reliance on Netlist's "proposed construction" is from another proceeding rather than the "plain and ordinary meaning" construction it asserts now. *Id.*

The Court agrees with Netlist. As noted *supra*, "CAS latency" is not limited to only a "read latency," see Part IV.K., which negates Micron's first argument. Micron's second argument—that registering data being transferred through the circuitry could never make a zero delay greater than anything—relates to infringement rather than indefiniteness. While it may be true that, under Netlist's interpretation of "CAS latency," the recited limitation can never be met by an accused device, that does not mean the term is indefinite—only that infringement is impossible. The Court therefore holds Micron has not carried its burden of showing this term is indefinite.

V. CONCLUSION

The Disputed Terms	The Court's Construction
The "Rank" Terms ('912 Patent, '417 Patent, '215 Patent)	A "rank" of memory is "a 'bank' of one or more devices on a memory module that operate in response to a given signal"
"signal" / "row [/column] address signal" ('912 Patent, all claims)	Plain and ordinary meaning

"A memory module connectable to a computer system, the memory module comprising" ('912, preamble to all asserted claims) "A memory module operable to communicate with a memory controller via a memory bus, the memory bus including signal lines, the signal lines including a set of control/address signal lines and a plurality of sets of data/strobe signal lines, the memory module comprising: ('608 Patent, Claim 1)	The preambles are limiting.
The Data Buffer Control Terms ('215 Patent, Claims 1, 21; '417 Patent, Claim 1)	The claims do not require a "fork-in-the-road" approach.
"logic" ('417 Patent, Claim 1; '215 Patent, Claim 1)	Plain and ordinary meaning
"circuitry" ('417 Patent, Claims 1, 6, 11)	Plain and ordinary meaning
"the at least one of the circuit components" ('215 Patent, Claim 15)	"the circuit components"
"burst of data strobe signals" ('215 Patent, Claims 12, 13, 28, 29)	Plain and ordinary meaning
"operable in a computer system to communicate data" ('215 Patent, Claim 1;'417 Patent, Claim 1)	Plain and ordinary meaning
"data buffer control signals" ('417 Patent, Claims 1, 3, 11)	Plain and ordinary meaning
"overall CAS latency" of a memory module ('417 Patent, Claim 1; '215 Patent, Claims 3, 4, 24, 25)	"the delay between (1) the time when a command is executed by the memory module, and (2) the time when data is made available to or from the memory module"
"actual operational CAS latency" of a memory device ('417 Patent, Claim 1)	"the delay between: (1) the time when a command is executed by the memory device, and (2) the time when data is made available to or from the memory device"

"actual operational CAS latency" of a memory integrated circuit ('215 Patent, Claims 3, 4, 24, 25)	"the delay between: (1) the time when a command is executed by the memory integrated circuit, and (2) the time when data is made available to or from the memory integrated circuit"
"wherein data transfers through the circuitry are registered for an amount of time delay such that the overall CAS latency of the memory module is greater than an actual operational CAS latency of each of the memory devices" ('417 Patent, Claim 1)	Plain and ordinary meaning

The Court **ORDERS** each party not to refer, directly or indirectly, to its own or any other party's claim-construction positions in the presence of the jury. Likewise, the Court **ORDERS** the parties to refrain from mentioning any part of this opinion, other than the actual positions adopted by the Court, in the presence of the jury. No party may take a position before the jury that contradicts the Court's reasoning in this opinion. Any reference to claim construction proceedings is limited to informing the jury of the positions adopted by the Court.

So ORDERED and SIGNED this 21st day of November, 2023.

RODNEY GILSTRAP
UNITED STATES DISTRICT JUDGE